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(54) ADDRESS DESIGNATION SYSTEM

(57) Abstract:

PURPOSE: To reduce the program quantity by dividing the general-purpose register which stores the operand and address modifying data for the arithmetic object into plural patial registers featuring a short bit number each and then performing the alteration for the register contents with a small amount of the order.

CONSTITUTION: The address designation is given to memory 11 according to the contents of data buffer 13, and the contents of buffer 13 is written into the address position designated by the contents and then read out from memory 11 to be stored in buffer 13. At the same time, the order in the contents of buffer 13 is set to order register 14, and the contents of register 14 is decoded via decoder 15. Then the contents of buffer 13 is applied to arithmetic registers 17 and 18 as well as to arithmetic circuit 19 and then supplied to general-purpose registers 21 and 22 after calculation. Registers 21 and 22 are divided into plural partial registers featuring the bit number same as or shorter than the data length of circuit 19. And the designation of different positions is secured for registers 21 and 22 according to the contents of the address.